Updated S 09/769,918

21	8	((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 with state$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:29
22	39433	diagnos$6 same state$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
23	9	((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 same state$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
24	1	(((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 same state$1)) not (((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 with state$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
25	4468756	plural$6 or mult$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:32
26	21323	(remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:36
27	3287	(plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:37
28	20943	power$6-down or power$6-up	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:38
29	137	((plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))) and (power$6-down or power$6-up)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:38
30	25	(((plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))) and (power$6-down or power$6-up)) and (710/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:39

Updated S 09/769,987

21	8	((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 with state$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:29
22	39433	diagnos$6 same state$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
23	9	((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 same state$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
24	1	(((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 same state$1)) not (((client$1 same (server$1 same (database$1 or (data adj base$1))) same access$6 same diagnos$6) and characteristic$) and (diagnos$6 with state$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 12:33
25	4468756	plural$6 or mult$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:32
26	21323	(remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:36
27	3287	(plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:37
28	20943	power$6-down or power$6-up	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:38
29	137	((plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))) and (power$6-down or power$6-up)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:38
30	25	(((plural$6 or mult$6) same ((remov$6 or alter$6 or insert$6 or add$6 or plug$6) same (memory near2 (card$1 or cartridge$)))) and (power$6-down or power$6-up)) and (710/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/14 15:39

US-PAT-NO: 5974554

DOCUMENT-IDENTIFIER: US 5974554 A

TITLE: Computer system with automatic configuration capability for industry standard architecture(ISA) cards

---------- KWIC ---------

Brief Summary Text - BSTX (6):

Computer systems may be provided with provisions for **adding** devices thereto. For example, an ISA (Industry Standard Architecture) type personal computer system may be provided with expansion slots coupled to the ISA system bus for receiving expansion device cards which **plug** into such expansion slots. Other types of expansion techniques may also be used, such as PCI (Peripheral Component Interconnect) slots, PCMCIA (Personal Computer **Memory Card** Interface Association) slots, Micro Channel slots, EISA slots, orthelike. Examples of such expansion devices include keyboard controllers, hard drive controllers, floppy drive controllers, video controllers, modems, network cards, **add-on memory cards, multimedia** cards, sound cards, I/O devices, or the like. An expansion device may comprise one or more logical devices each of which may be assigned system resources such as an I/O **address,** interrupt level, and DMA channel.

Brief Summary Text - BSTX (9):

In a first kind of PnP compatible ISA PC system, software stored in its ROM BIOS may configure a system after power up to assign system resources such as memory space, I/O addresses, interrupt levels, and DMA channels to each PnP ISA expansion card plugged in the system. The PnP ISA expansion cards built according to the PnP ISA specification may operate in conjunction with such software stored in the BIOS (i.e., PnP BIOS). In such a PC system, when power is applied to the system, PnP expansion cards required for system boot may become active on power up using **power-up** default system resources. Examples of

the devices required for system boot may include hard and floppy disc drive controllers, keyboard controllers, display controllers or the like. Other PnP ISA devices not required for system boot may power up in an inactive state. Examples of PnP devices not required for system boot may include modems, sound cards, or the like. Such devices may not be required for system boot and initial loading of operating system and the like.

Detailed Description Text - DETX (7):

In accordance with the proposal of the PnP ISA specification Version 1.0a (May 5, Dec. 10, 1994), all PnP device cards used in the computer system of this embodiment have four PnP card states, that is, Wait for Key, Sleep, Isolation, and Config states. After a **power-up** reset, or in response to the Reset and Wait for Key commands, all cards enter the Wait for Key state. No commands are active in this state until the initiation key is detected on the ISA bus 10. This state is the default state for PnP cards during normal system operation. After configuration and activation, PnP software return all cards to this state.

Current US Cross Reference Classification - CCXR (1):

710/104

US-PAT-NO: 5938750

DOCUMENT-IDENTIFIER: US 5938750 A
See image for Certificate of Correction

TITLE: Method and apparatus for a memory card bus design

---------- KWIC ---------

Brief Summary Text - BSTX (10):
In FIG. 1, the microcontroller 160 executes instructions received from the host computer by execution of a sequence of corresponding instructions stored in program memory device 165, therefore, microcontroller 160 is continuously powered up to perform operations required to support the PCMCIA operations. Accordingly, the PCMCIA card 100 consumes a relatively large amount of power in the host computer because the microcontroller is continuously in a **powered-up** state.

Detailed Description Text - DETX (7):
The interface signals further include two voltage detection signals, the voltage sense 1 signal (VS1) and the voltage sense 2 signal (VS2), which allow the host to determine the **power-up** voltage for the Miniature Card. The VS1 signal and the VS2 can be sensed by a multiple-voltage hosts to determine the card's power requirements. These signals are similar to those found in PCMCIA cards.

Claims Text - CLTX (11):
5. The **insertable memory card** of claim 1, wherein the **insertable memory card comprises multiple memory** devices.

Current US Original Classification - CCOR (1):
710/301

Current US Cross Reference Classification - CCXR (1):
710/13

US-PAT-NO: 5935252

DOCUMENT-IDENTIFIER: US 5935252 A

TITLE: Apparatus and method for determining and setting system device configuration relating to power and cooling using VPD circuits associated with system devices

---------- KWIC ---------

Detailed Description Text - DETX (4):
As mentioned at the outset, an enhanced way of determining device characteristics is provided. Information circuits are **added** to system processors, backplanes, and **memory cards** of a computer system to provide configuration and asset information. A preferred embodiment of the invention uses smart card VPD chips. These smart card VPD chips provide secure, i.e., encrypted, data storage, and communicate using half-duplex, asynchronous block protocol, such as described in the international communication standard, ISO 7816-3. However, this communications standard provides limited addressability and, for that reason, and in consideration of electrical loading and performance reasons, a large number of smart card VPD chips cannot be connected to a common, **multi**-dropped interface. Further, since failures on a **multi**-dropped interface can preclude communication with all chips, and since communication with a subset of the VPD chips 120 is required to successfully operate the system, a more robust design uses point-to-point interlaces. This in turn creates the need to concentrate a large number of point-to-point interfaces to a common transfer point for communication with the system. A way of concentrating the signals from the VPD chips 120 to a control point, and further a way of handling the special protocol requirements of the VPD chips 120 within an existing system's network protocol, e.g., SPCN, are the subject of the related co-pending application attorney docket number RO997-084-IBM-102, referenced above.

Detailed Description Text - DETX (37):
The process begins when a system power on request is initiated by

the system operator. Power is applied to the VPD chips 120 and concentrator 116. Simultaneously, SPCN starts the **power-up** sequence and the panel 106 begins collection of VPD for the first 15 ports.

Detailed Description Text - DETX (38):
FIG. 5 illustrates the process of retrieving the power VPD table, analyzing the contents and configuring the power system. At a point early in the **power-up** sequence, SPCN issues a command to the panel 106 requesting the power VPD table. If the table cannot be successfully received, the **power-up** fails and a fault is displayed. If the command is successful, SPCN examines the value in the "max index" field in the first entry of the table. If this field contains zero, then no VPD was retrieved by the panel 106, the **power-up** is aborted and a fault is displayed. If the "max index" contains a non-zero value, the process continues to analyze the processor and backplane VPD, which are further illustrated in FIGS. 6 through 9. After analysis of the VPD, the "vpd level mismatch" flag is examined. This flag indicates that all the required VPD was not available and consequently, some parameters will be set to default values. A fault is displayed to indicate the problem. The configuration data determined from the VPD analysis in FIGS. 6 to 9 is applied to the power and cooling functions.

Detailed Description Text - DETX (39):
FIG. 6 illustrates the process of analyzing processor power VPD. If processor 1 is present and, if the power VPD was successfully retrieved as determined by the Header Flag byte in the first processor entry, the processor VPD is examined as illustrated by FIG. 7. After processor 1 VPD is analyzed, the power VPD for processors 2 and 3, if available, are matched against processor 1. If the power VPD from all processors does not mach, the **power-up** is failed and a fault is displayed.

Detailed Description Text - DETX (40):
If VPD for processor 1 is not available, then the processor 2 entry is examined. If the VPD for processor 2 is available, the processor VPD is examined as illustrated by FIG. 7. After processor 2 VPD is analyzed, the VPD

for processor 3, if available, is matched against processor 2. If the power VPD from both processors does not match, the **power-up** is failed and a fault is displayed.

Detailed Description Text - DETX (41):
If VPD for processor 2 is not available, then the processor 3 entry is examined. If the VPD for processor 3 is available, the processor VPD is examined as illustrated by FIG. 7. If no processor VPD is available, then the **power-up** attempt is failed and a fault is displayed.

Detailed Description Text - DETX (43):
Invalid cache parameters cause the **power-up** to fail to protect circuit components. Invalid cooling configuration causes all blowers to be set to their maximum speed, and the **power-up** sequence continues.

Detailed Description Text - DETX (44):
FIG. 8 illustrates the process of determining if SPCN code is at the correct level to be able to correctly interpret the power VPD data. The high nibble of byte 34 contains the critical VPD code level. The corresponding parameter in the SPCN code must be numerically equal or greater, or the **power-up** is failed and a fault is displayed. This indicates that the SPCN code may not be sufficiently current to interpret all the fields of the VPD data and consequently circuit damage conditions could exist.

Detailed Description Text - DETX (45):
The low order nibble of byte 34 contains the non-critical or functional level of the VPD data. The corresponding parameter in the SPCN code must be numerically equal or greater to correctly interpret the VPD data, but no circuit damage conditions exist. The **power-up** is not cancelled, but a fault is displayed because the power/cooling/concurrent maintenance system may be incorrectly configured.

Detailed Description Text - DETX (46):
FIG. 9 illustrates the process of analyzing backplane power VPD. The Header, FRU type, and VPD level are examined in the same manner as for the

processor, however, if failures are detected, the **power-up** sequence is not
cancelled as no damage conditions exist. The backplane specific power VPD in
byte 36 is examined to extract additional configuration parameters.

Detailed Description Text - DETX (47):

FIGS. 10 and 11 illustrate the process used by the panel 106 to collect VPD
from the first 15 ports. This is the amount required by the power controller
(SPCN) to configure the power system and complete the **power-up** sequence. The
panel 106 proceeds to collect the remainder of the VPD after SPCN signals that
the **power-up** sequence has completed successfully add that collection is
identical to the process illustrated in FIGS. 10 and 11. The specific commands
required to communicate with the concentrator 116 and the smart card VPD chips
120 are not pertinent to this disclosure.

Current US Cross Reference Classification - CCXR (1):

710/104

US-PAT-NO: 5892972

DOCUMENT-IDENTIFIER: US 5892972 A

TITLE: Method of constructing a plug and play compatible bus card which allows for mass production of the bus card

---------- KWIC ---------

Brief Summary Text - BSTX (8):

The plug and play specification requires each bus card to have a unique identification number (the "ID") in order to automatically configure an ISA bus card. This ID is read by a host processor at the time of **power-up** or system reset to configure the device. Additionally, to comply with the plug and play standard, the ISA bus card must store its system resources (resource data structure, or "RDS") on the card itself. It is recommended in the plug and play specification that the ID and the system resources (RDS) be stored in serial electrically erasable programmable read only memory (EEPROM).

Brief Summary Text - BSTX (15):

A further aspect of the invention provides a method of retrieving information from a bus card that is compatible with a **plug** and play protocol, the bus card having a random access memory that stores an identification unique to the bus card, a read only memory that stores resource data common to a **plurality** of bus cards, and a processor. The method comprises examining an **address** provided to the processor in a request for information from the bus card. The processor retrieves the identification from the random access **memory of the bus card when the address** indicates that the information requested is the identification for that bus card. The processor retrieves the resource data from the read only **memory of the bus card when the address** indicates that the information requested is the resource data. In certain embodiments, the identification is retrieved when the **address** is within a first portion of a memory space of the bus card, and the resource data is retrieved when

the
address is not within the first portion of the memory space of the bus card.

Current US Original Classification - CCOR (1):
710/8

Current US Cross Reference Classification - CCXR (1):
710/10

Current US Cross Reference Classification - CCXR (2):
710/104

US-PAT-NO: 5634075

DOCUMENT-IDENTIFIER: US 5634075 A

TITLE: Backward compatibility for plug and play systems

---------- KWIC ---------

Abstract Text - ABTX (1):

A device for use in a computer system, particularly a personal computer (PC) which provides compatibility for a proposed ISA plug and play (PNP) standard. The device of the present invention is also backward compatible with non-PNP (legacy) PCs. Upon **power-up,** a device may initialize using default traditional or specification (ISA) values for I/O address, IRQ and DMA channels. If PNP activity by the host PC is detected by the device, the device is disabled, and awaits activation and I/O address, IRQ and DMA channel assignments from a host PC. If no PNP activity by a host PC is detected, the device continues to operate using default traditional or specification (ISA) I/O address, IRQ and DMA channels. The device of the present invention may be installed in PNP or legacy type PCs without reconfiguring hardware (e.g., DIP switches, jumpers or the like) in the device or installing new firmware, operating system, or applications software in a host PC.

Brief Summary Text - BSTX (5):

Examples of devices which may be **added** to a computer through expansion slots or the like include modems, network cards, **add-on memory cards, multimedia** cards, sound cards (e.g., Soundblaster.TM. card or the like), hard drive and/or floppy drive controllers, I/O devices or the like. A device may comprise one or more logical devices, each of which may be assigned system resources such as an I/O **address,** interrupt level, and DMA channel. Devices may also be provided on the PC system motherboard, such as internal memory, keyboard controller, hard and floppy drive controller, video controller, or the like, and may also be assigned I/O **addresses,** interrupt levels, and DMA channels. For the purposes of this application, the term "device"

shall refer
to such **add** on or internal devices for a PC.

Brief Summary Text - BSTX (10):

It may be possible to reconfigure a PC or a device to overcome such a problem. For example, software may be provided with an expansion device to reconfigure the PC after power up to alter the predetermined I/O addresses, interrupt levels, and DMA channels. A user may install such software in a PC to operate upon **power-up** or reset (e.g., as an AUTOEXEC.BAT file or as a device driver in a CONFIG.SYS file) to reconfigure default I/O addresses, interrupt levels, and/or DMA channels in the ROM BIOS of a PC. Alternately, the device may be altered by use of jumper blocks, DIP switches, or the like, to reconfigure the device to use a different I/O address, interrupt level, and/or DMA channel.

Brief Summary Text - BSTX (15):

In step 100, power is applied to a PC. In step 113, PNP devices required for system boot may become active on power up using **power-up** default I/O addresses, interrupt levels, and DMA channels. Examples of devices required for system boot may include hard and floppy disc drive controllers, keyboard controllers, display controllers (e.g., VGA controller) or the like. For a system booting off a network (e.g., Novell.TM. type network) a network card may be considered a device required for system boot. Default I/O addresses, interrupt levels, and DMA channels may be preassigned and may be those addresses used under the current ISA (i.e., non-PNP) standard or traditional industry addresses.

Brief Summary Text - BSTX (37):

A multiplexer generates a high level logic signal as a device enable signal upon reset and **power-up**. The multiplexer has another input coupled to the system data bus and receives a signal characteristic of a computer system attempting to enable a device after assigning an I/O address. The multiplexer receives as a switching signal the comparison signal from the comparator.

Brief Summary Text - BSTX (39):
A DMA channel register stores a DMA channel for the device. The DMA channel
register is configured to output a default DMA channel on **power-up**. The
control logic, upon detecting activity on the computer system data bus characteristic of a computer system attempting to assign a DMA channel to a
device, allows a computer system to write to the DMA channel register a DMA
channel.

Brief Summary Text - BSTX (40):
An interrupt level register stores an interrupt level for the device. The
interrupt level register is configured to output a default interrupt level on
power-up. The control logic, upon detecting activity on the computer system
data bus characteristic of a computer system attempting to assign interrupt
level to a device, allows a computer system to write to the interrupt level
register an interrupt level.

Claims Text - CLTX (2):
first storage means, coupled to said computer system data bus, for storing
an I/O address for the device, wherein said first storage means outputs a
default I/O address upon **power-up**;

Claims Text - CLTX (3):
a DMA channel register, coupled to said computer system data bus, for
storing a DMA channel value for the device, wherein said DMA channel register
outputs a default DMA channel value upon **power-up**;

Claims Text - CLTX (4):
an interrupt level register, coupled to said computer system data bus, for
storing an interrupt level value for the device, wherein said interrupt level
register outputs a default interrupt level value upon **power-up**; and

Claims Text - CLTX (14):
a multiplexer, coupled to a high level logic signal, for generating a high
level logic signal as a device enable signal upon reset and **power-up**, said
multiplexer having another input coupled to said system data bus for

receiving
a signal characteristic of a computer system attempting to enable a device
after assigning an I/O address, said multiplexer receiving as a switching
signal said comparison signal from said comparator.

Claims Text - CLTX (20):
storing, in a first storage means coupled to said computer system data bus,
a default I/O address upon **power-up**;

Claims Text - CLTX (21):
storing, in a DMA channel register coupled to said computer system data bus,
a default DMA channel value upon **power-up**;

Claims Text - CLTX (22):
storing, in an interrupt level register coupled to said computer system data
bus, a default interrupt level value upon **power-up**;

Current US Original Classification - CCOR (1):
710/9

Current US Cross Reference Classification - CCXR (1):
710/302

US-PAT-NO: 5572683

DOCUMENT-IDENTIFIER: US 5572683 A
See image for Certificate of Correction

TITLE: Firmware selectable address location and size for cis byte and ability to choose between common memory mode and audio mode by using two external pins

---------- KWIC ---------

Abstract Text - ABTX (1):

An interface card has an interface logic block for interfacing a peripheral device with a computer host and for selecting either a common memory mode or an audio mode where the computer host can enable or disable a common memory read or write operation in the common memory mode. In the common memory mode, the computer host can choose to read card information service (CIS) bytes internally or externally. The interface logic block has, (a) a first external pin used either for a common memory chip select (CMCS) signal in the common memory mode or for an audio-in (AudIn) signal for the audio mode, (b) a second external pin used either for a common memory write (CMWR) signal in the common memory mode or for an audio-out (AudOut) signal in the audio mode, (c) a **plurality** of registers, (d) a logic circuit coupled to the registers, and (e) a microcontroller which can enable or disable the common memory write operation. The registers further include a configuration option register (COR), a card configuration and status register (CCSR), a pin replacement register organization (PRRO), a **memory card address** register, a **memory card** data register and an interface configuration register (ICR). Attribute memory range select bits in the ICR allow firmware selectable attribute memory locations of CIS bytes, the COR, CCSR and PRRO.

Detailed Description Text - DETX (19):

Some registers in interface logic block 1 are asynchronous. These registers include a configuration option register (COR), a card configuration and status register (CCSR) and an interface configuration register (ICR). These

registers will be discussed in detail later. During a **power-down** mode, because the clock unit stops sending the clock pulses, the various components in main interface unit 3 cannot follow the clock pulses. Because the COR, CCSR and ICR need to be accessed at all times whether interface card 4 is in a **power-down or power-up** mode, these registers operate asynchronously. The registers use master-slave latches in which, for example, if a write signal is sent to interface logic block 1, the write signal is used as a clock signal, and the data is latched when the write signal arrives. Thus, these registers operate asynchronously with respect to time other components in main interface unit 3.

Detailed Description Text - DETX (42):
Continuing to refer to FIG. 7, AudioEn 54 is an audio enable bit. In order for an audio signal to be sent to host 1000, host 1000 has to set AudioEn 54 bit. PD 55 is a **power-down** bit used by host 1000 to request that interface card 4 to go into a **power-down** mode. During a **power-down** mode, all I/O access via IORD#14 and IOWR#15 are ignored. However, an access to COR 35 in FIG. 6, CCSR 50 in FIG. 7 or PRRO 60 in FIG. 8 is still allowed during the **power-down** mode. INTR 56 is an interrupt bit used to determine if an interrupt is pending (1) or not (0). The value is available whether or not the interrupts have been configured. The description of CCSR 50 bits is summarized in Table 2.

Detailed Description Text - DETX (44):
Now referring to FIG. 8, pin replacement register organization (PRRO) 60 mentioned above is described in detail. The lower four bits of PRRO 60 are written by microcontroller 2 and may be read by both host 1000 and microcontroller 2. Rdy/Bsy#67 is a ready-or-busy signal bit, indicating whether interface card 4 is ready or busy. Upon **power-up,** Rdy/Bsy#67 is 0, and CE 42 in FIG. 6 is also set to 0. This causes IRQ#20 in FIG. 2 to be 0. Microcontroller 2 has a responsibility of setting Rdy/Bsy#67 to let host 1000 know that interface card 4 is ready to be used. The upper bits of PRRO 60 are delta bits. Any of the four bits can be set if the corresponding lower bit has

US-PAT-NO: 5038320

DOCUMENT-IDENTIFIER: US 5038320 A

TITLE: Computer system with automatic initialization of pluggable option cards

---------- KWIC ---------

Abstract Text - ABTX (1):

A data processing system includes a planar board having a central processing unit (CPU), a main memory unit, and input/output (I/O) sockets or slots, each adapted to receive a selected one of a plurality of different and/or similar option cards. each card contains (or is connected to) and controls a respective peripheral device; and each card is pre-wired with an ID value corresponding to its card type. Software programmable option registers on each card store parameters such as designated default (or alternate) address information, priority levels, and other system resource parameters. A setup routine, during initial power-on, retrieves and stores the appropriate parameters in the I/O cards and also in slot positions in main memory, one position being assigned to each slot on the board. Each slot position is adapted to hold the parameters associated with the card inserted in its respective slot and the card ID value. That portion of main memory containing the slot positions is adapted to maintain the parameter and ID information by means of battery power when system power fails or is disconnected, i.e., a nonvolatile memory portion. Subsequent power-on routines are simplified by merely transferring parameters from the table to the card option registers if the status of all the slots has not changed since the last **power-down,** system reset, or channel reset.

Brief Summary Text - BSTX (2):

Users of smaller computer systems typically do not have sophisticated programming skills, and user-transparent programmable parameter switches have been suggested to simplify configuration of the systems to the user's needs. However, the routines that are required to so configure such systems are

complex, error prone, and time consuming. It is an objective of the present improvement to substantially reduce the time delay experienced by a user before he can do productive work on the system upon re-powering or resetting of the system after a **power-down,** so long as no cards are changed in, added to, or removed from the slots.

Brief Summary Text - BSTX (8):

However, if after a **power-down,** no change is made in the cards attached to the slots or in the slot positions of the cards, a simplified setup routine determines that no change has been made by comparing each card ID with the ID value stored in the respective slot position. Then the routine transfers the parameter data from the memory slot positions to the respective card registers; and the system is ready for normal operation.

Detailed Description Text - DETX (6):

A feature to be described is the use of this information in the nonvolatile memory to speed up initialization (FIG. 7) of the system when the slot configuration has not changed since the last **power-down,** and thereby reduce the time the user has to wait to begin useful applications after operating the system power-on switch, not shown, or after system or channel reset. This difference in complexity and number of steps required is illustrated by FIGS. 6 (initialization) and 7 (POST).

Detailed Description Text - DETX (8):

Register 21 stores parameter information for controlling communications between the card and the system, including the address factor AD, the priority value PR, the state bit S, and other information O described with respect to module 10. This information is set by the central system during **power-up** initialization (FIG. 6). A feature of the system is that, if slot conditions have not changed since the last **power-down** of the system, the information is simply transferred to register 21 from the nonvolatile memory 10 in a relatively fast operation (FIG. 7), whereas if slot conditions have changed the system is required to perform a lengthy program process (FIG. 6) to retrieve

and/or develop some or all of the information and then transfer it to both memory 10 and the card register 21.

Detailed Description Text - DETX (9):

Control logic 22 and decode logic 23 control response of the card 5-7 to I/O addresses appearing on bus 17. When power is applied to the system, the cards are addressable initially only through their sockets, and a portion of the address bus. But after the **power-up** process, the value AD in register 21 controls decoder 23 to detect a default or alternate I/O address associated uniquely to the card type and unrelated to the socket location. Upon such detection, the priority value PR and state bit S in conjunction with control logic 22 determine when data may be exchanged between the card and the bus 17. One manner in which an AD value, the decoder 23 and logic 22 detect an I/O address is shown and described in Interfacing to the IBM Personal Computer by L. Eggebrecht published 1983 at pages 130, 131.

Detailed Description Text - DETX (10):

In operation, during its **power-up** sequence the central system individually addresses the option sockets, by sending respective "slot address" signals on the bus which are uniquely detected by decoder 14 and result in separate activation of setup (or enable card) lines EC0-EC7 extending to respective sockets 2-0 to 2-7 and through the sockets to attached cards 5-0 to 5-7. Upon activation of one such line, if the respective socket is vacant the hexadecimal value of FFFF is returned to the system which terminates further operation relative to that socket. However, if the socket contains a card, the activated line in conjunction with additional address signals on the bus 17 condition logic 22 on the respective card to cause drivers 20 to transmit the ID signals mentioned above which identify the respective card and device type. The system CPU compares the returned ID signals with the ID value stored in the location in memory 10 allocated to the respective slot, and sets an indication denoting whether the compared values are the same or different. This indication serves

effectively as a branch condition for subsequent program processes which determine the action to be taken relative to the respective slot.

Detailed Description Text - DETX (12):

Mismatching comparisons occur when the state of the interrogated socket has been altered. The ID value stored in memory 10 relative to a socket which was vacant at last **power-down** is FFFF, and the ID value stored relative to a previously occupied socket is that of the card last occupying that slot. Thus, if a card is installed into a previously vacant slot or substituted for a card having a different ID, a mismatching comparison will occur causing the system to retrieve and/or develop new AD, PR, S, and O values for the responding card.

Claims Text - CLTX (5):

2. A data processing system having a plurality of I/O sockets for attaching cards of different types, and in which the system during subsequent **power-up** retrieves parameter data for at least one card currently attached to the system by way of a respective socket and in which means is provided on the card for permanently storing an identity value corresponding to the card type, said system comprising;

Claims Text - CLTX (7):

means effective upon **power-up** of the system for comparing the identity value stored on the attached card with the identity value stored in the nonvolatile memory location corresponding to the socket to which the card is attached; and

Claims Text - CLTX (12):

said comparing means further effective upon **power-up** of the system for comparing the null identity value produced upon interrogating an empty socket with the identity value in the nonvolatile memory location corresponding to that socket for determining if that socket had contained a card when the system previously was powered down.

Claims Text - CLTX (19):

said comparing means further effective upon **power-up** of the system for comparing the predetermined identity value produced upon interrogating an empty socket with the identity value in the nonvolatile memory location corresponding to that socket for determining if that socket had contained a card when the system previously was powered down.

Claims Text - CLTX (45):

10. In a data processing system comprising one or more processing units, one or more memory units, I/O sockets for attachment of peripheral option cards, and an I/O bus interconnecting said units with each other and with said sockets for transferring information between said units and between cards attached to said sockets and said units, each said socket at any time having a condition of being either vacant or occupied by any of a **plurality** of different types of option **cards, each of said memory** units and sockets having a predetermined **address** on said bus, the improvement comprising:

Claims Text - CLTX (62):

15. A data processing system having a plurality of I/O sockets for attaching cards of different types, and in which the system during an initial **power-up** creates parameter data for at least one card currently attached to the system by way of a respective socket and in which means is provided on the card for permanently storing an identity value corresponding to the card type, said system comprising:

Claims Text - CLTX (64):

means effective upon **power-up** of the system for comparing the identity value stored on the attached card with the identity value stored in the nonvolatile memory location corresponding to the socket to which the card is attached; and

Current US Original Classification - CCOR (1):

710/10

Current US Cross Reference Classification - CCXR (1):

710/12